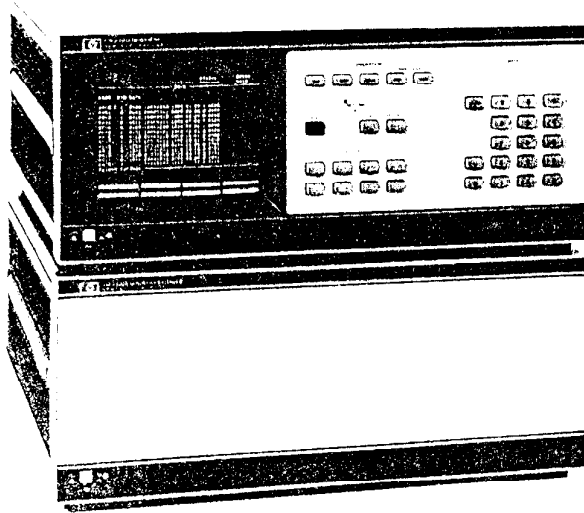# DATA GENERATORS & DATA ANALYZERS
## Data Generator/Analyzer System
Models 8180A, 8181A, 8182A

- Digital ac parametric and functional characterization
- 50 MHz, 1 kbit/channel
- Direct measurements, 100 ps/10 mV resolution

- Variable sampling point delay in synchronous operation
- Real-time data comparison
- Convenient softkey operating concept with live keyboard

Upper: HP 8180A Data Generator
Lower: HP 8181A Data Generator Extender
Up to 64* channels with HP 8180A and two 8181A's.
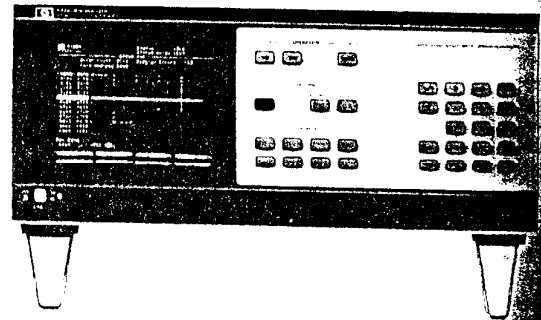
HP 8182A Data Analyzer (up to 32* channels)

*Number of channels can be doubled by parallel operation.

An Affordable Engineering Tool for At-Speed Characterization of Digital Hardware.

This compact, benchtop system is designed for manual and automatic engineering investigations on all types of digital hardware. It also upgrades ATS to at-speed testing. Features such as the same high resolution for generator and analyzer, and matched control signals, guarantee the viability of these measurements. Modularity promotes cost-effectivity because the number of channels can be increased without loss of speed or memory.

The same guided operating concept speeds familiarization, and common HP-IB syntax and free format accelerate programming. Live keyboards give rapid parameter access without changing software. Data entry is simplified by the predefined patterns and extensive edit features. Mixed logic needs are solved because up to 6 different levels can be assigned to any number of individual channels.

Data Generator

Timing capabilities include individual delay and width on two clock channels for dual-phase applications, and on RZ data channels for setup and hold time measurements. HP 8181A Extender group delay allows separate timing of e.g. simulated address signals.

High-speed pulses and clean shape provide performance for all common logic. Variable, high resolution levels allow worst-case conditions to be measured. The segmentable memory allows initialization and looping of data (upon an external signal) to be set up.

Data Analyzer

In addition to at-speed analysis, comparison and glitch detection, the HP 8182A also measures multichannel output timing like propagation delays because the sampling point is variable. For investigations in e.g. the setup/hold interval, a real-time compare mode examines data stability throughout a programmable window: any deviation from the expected state is displayed and error signals permit operations such as 'stop on error' for trapping sporadic faults.

Specifications

Specifications apply for operating temperatures from 0°C to

HP 8180A/8181A Data Generator/Extender
Memory and Channels
Memory depth: 1024 bit/channel
Number of channels: up to 64 using HP 8180A with two HP Extenders. Up to 128 channels with 2 sets of equipment in operation.
HP 8180A Channels
RZ (return-to-zero) channels: independent variable width in each of up to 8 channels.
NRZ (non-return-zero) channels: Up to 16 channels, number of RZ channels. Fixed timing.
Strobe channel: NRZ data or clock. Fixed timing
Clock channels: independent delay and width in each of Clock 1 can be selected to run continuously in Break state modes').
HP 8181A Channels
NRZ: up to 24 channels. Fixed timing within an Extender lay with respect to HP 8180A.
Memory Loading
Codes: bin, oct, hex, dec (address codes: oct, hex, dec)
Entry: Keyboard or HP-IB.
Displayed channel order: user-defined.
Line edit: insert, delete, macro.
Channel edit: clear, set, copy, prbs, counts, entry ma

Cycle Modes
Single, Auto, Initialization + Auto, Gated, Initializa (Initialization data is output at the beginning of the fi
Break state: implemented by manual or external BRE or by strobe channel bit. Data is held at current addre external RUN command cause same cycle to continue

Modes (Cont.)

state: implemented by manual or external STOP command.
is held at current address and the cycle is terminated. Manual or
RUN command trigger a new cycle.

ming
period: 20 ns to 950 ms (1.05 Hz to 50 MHz). Ext clock 0 to
MHz.

(relative to strobe channel): 0.0 ns to 950 ms, max 90% period −18ns.
: 10.0 ns to 950 ms, max 90% period −8ns.
≤2ns for NRZ channels and RZ channels programmed for
delay.
olution: 3 digits (best case 100 ps).
uracy: ±5% of programmed value ±1ns.
≤0.2% + 100 ps (+ additional 50 ps for delay and width).

puts
ut impedance: 50 Ohm
and clock: 4 different high level / low level pairs can be defined
assigned to any number of individual outputs. Each channel has
endent normal / complement switching. Common 'off'.
-out: can be selected for 50 Ohm or high impedance load (com-
selection for all channels).

	50 Ohm load	High-impedance load
level:	−1.50 to +5.50 V	−1.00 to +17.0 V
level:	−2.00 to +5.00 V	−2.00 to +16.0 V
olution:	3 digits (10 mV)	−2.00 to +16.0 V
plitude:	0.5 to 5.5 V	3 digits (best case 20 mV)
sitions:		1.0 to 17 V
to 90%	(3 + |0.2 ampl |) ns	(3 + | 0.5 ampl |) ns
to 80% at ECL levels: 1.5 ns		

obe: ECL/TTL selectable

P 8182 Data Analyzer

mory and Channels
mory depth: 1024 bit/channel
mber of channels: up to 32. Can be doubled by parallel opera-
of two HP 8182A's.
pected data memory: 1024 bit/channel, segmentable.
Codes: bin, oct, hex (address code: dec).
Entry: Keyboard, HP-IB or read-in from DUT.
Displayed channel order: user-defined.
Line edit: word mask (don't care), insert, delete.
Channel edit: clear, set, copy, mask (don't care), exchange.

des
lysis / store-and-compare: synchronous sampling with varia-
analog sampling point delay or asynchronous sampling. Compari-
with expected data, if required.
Displays: state list, timing diagram, or error map.
litch detection: down to 5 ns. Memory depth is halved when
litch detection is selected.
Trigger condition: can be selected to start or stop analysis.
al-time compare: comparison of actual with expected data
oughout a time window. Window has variable analog delay and
th. Real-time and latched error output signals are provided.
Display: error map.
Trigger conditions: starts comparison.

ming
ternal clock: 0 to 50 MHz.
lay
(relative to external clock): 0.0 ns to 1 s, max 95% period - 1 ns.
ompare window width: 10.0 ns to 1 s, max 95% period - 9 ns.
annel skew: <2 ns
esolution: 3 digits (best case 100 ps).
ccuracy: ±5% of programmed value ±1 ns.
ternal clock: 1 Hz to 50 MHz (1-2-5) steps).

Inputs
Data: 6 different thresholds or dual threshold pairs can be defined and
assigned to any number of individual inputs.
Clock: programmable threshold and selectable slope (positive, nega-
tive, both).
Input Impedance: 1 MOhm, <7pF.
Control signals: (100 kOhm / 50 Ohm selectabel input impedance)
  Trigger arm and ext stop signals: independent programmable
  thresholds and selectable slope (positive, negative, don't care).
  Trigger qualifier and clock qualifier signals: independent
  programmable threshold and selectable levels (high, low, don't
  care).
Threshold range: −10.0 to +10.0 V.
Dynamic range: threshold ± 10 V.
Resolution: 3 digits (best case 10 mV).

Trigger
Trigger arm, word and qualifier, digital filter (1 to 16), clock and
qualifier, delay (0 to 65535).

Ordering Information

	Price
HP 8180A Data Generator* (includes 8 NRZ chan-nels)	$15,900
Opt 001 4 additional NRZ channels	$2,300
Opt 002 4 additional RZ channels	$5,500
HP 8181A Data Generator Extender (includes 8 NRZ channels)	$9,400
Opt 001 4 additional NRZ channels	$2,300
HP 8182A Data Analyzer* (includes 8 channels)	$15,800
Opt 001 8 additional channels	$5,100

*HP-IB cables not included

HP 8180A/8181A/8182A Accessories

HP 15406A 8182A clock probe (supplied)	$105
HP 15407A 8182A cable set with probes for 4 data channels (supplied)	$370
HP 15408A 5 plug-on grabbers with ground leads (sup-plied with 8182A and 15413A)	$75
HP 15409A 5 plug-on BNC adaptors	$75
HP 15410A 5 plug-on SMB adaptors	$75
HP 15411A 5 plug-on coax open-end adaptors	$75
HP 15413A Tri-State Pod	$60
Each Pod includes a set of grabbers (HP 15408A)	$850
HP 15414A Tri-State Unit 4-24 channels, levels programmable via 8180A/8181A, selectable inhibit conditions	$2120
HP 15415A 5 plug-on miniprobes (for HP 10024A IC test clip)	$75
HP 15416A cable for parallel operation of 2 each HP 8182A	$55
HP 15421A cable for parallel operation of 2 each HP 8180A	$55
HP 15422A 8180A cable set for clock 1, clock 2 and strobe (supplied)	$85
HP 15423A 8180A/81A cable set for 4 data channels (supplied)	$105
HP 15424A Performance Board	$1300
HP 15425A Test Head	$4300
HP 15426A 20 solder-in receptacles (supplied)	$70
HP 15427A DUT Board	$100
HP 15428A	$240
20 dual-in-line relays for use with HP 15425A Test Head, maximum current 250 mA	
HP 81800A Software Pac for series 200 controller	$1,300

Information

For more detailed information the following publications are avail-
able: Product Brochure (5952-9548), Application Note (5952-9549),
HP 8180A/81A Technical Data (5952-9550), HP 8182A Technical
Data (5952-9551), HP 15413A/14A Technical Data (5952-9556),
HP 15424A/25A Technical Data (5952-9562), HP 81800A Soft-
ware Pac (5952-9558), Ordering Guide (5952-9563).

Please refer also to chapter Components & Semiconductor Mea-
surement for detailed information of Digital Circuit Test System HP
81800S (page 369).